

**FAULTED
CONDITION
Prior art**

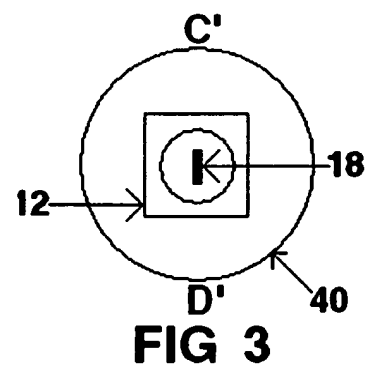
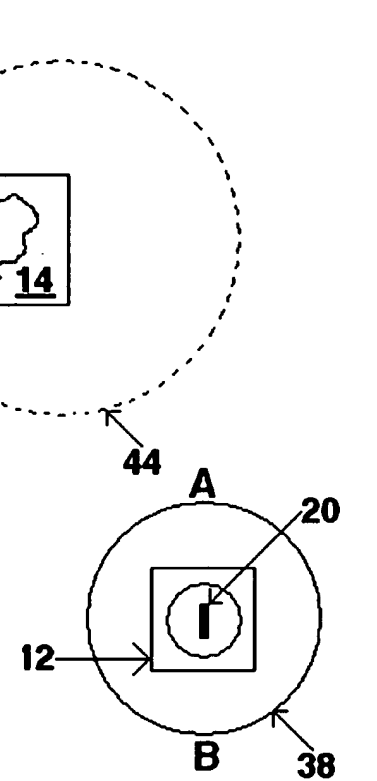
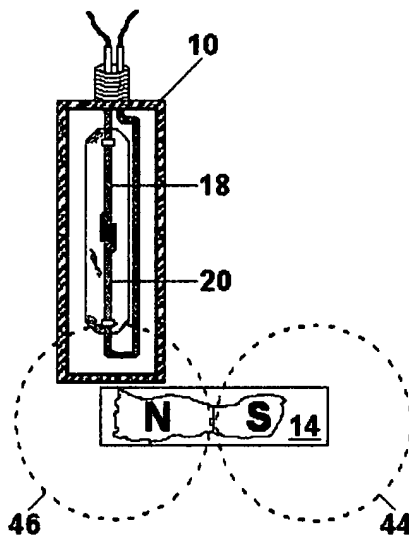


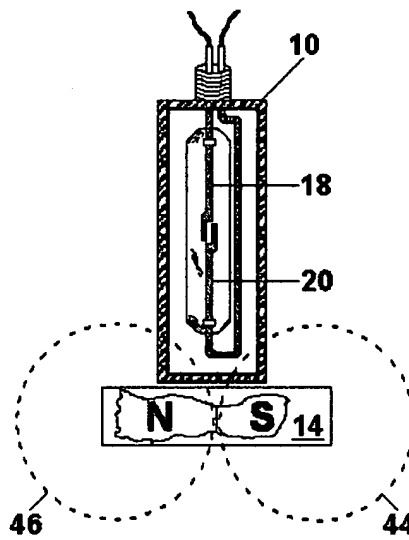
FIG. 1D



Prior Art

**Normal
Circuit**

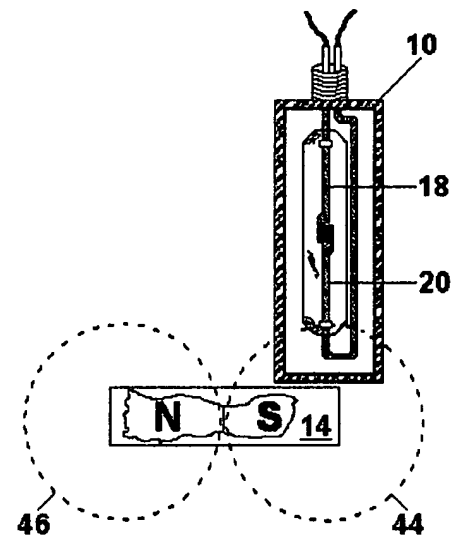
FIG. 1E



Prior Art

**Faulted
Circuit**

FIG. 1F



Prior Art

**Normal
Circuit**

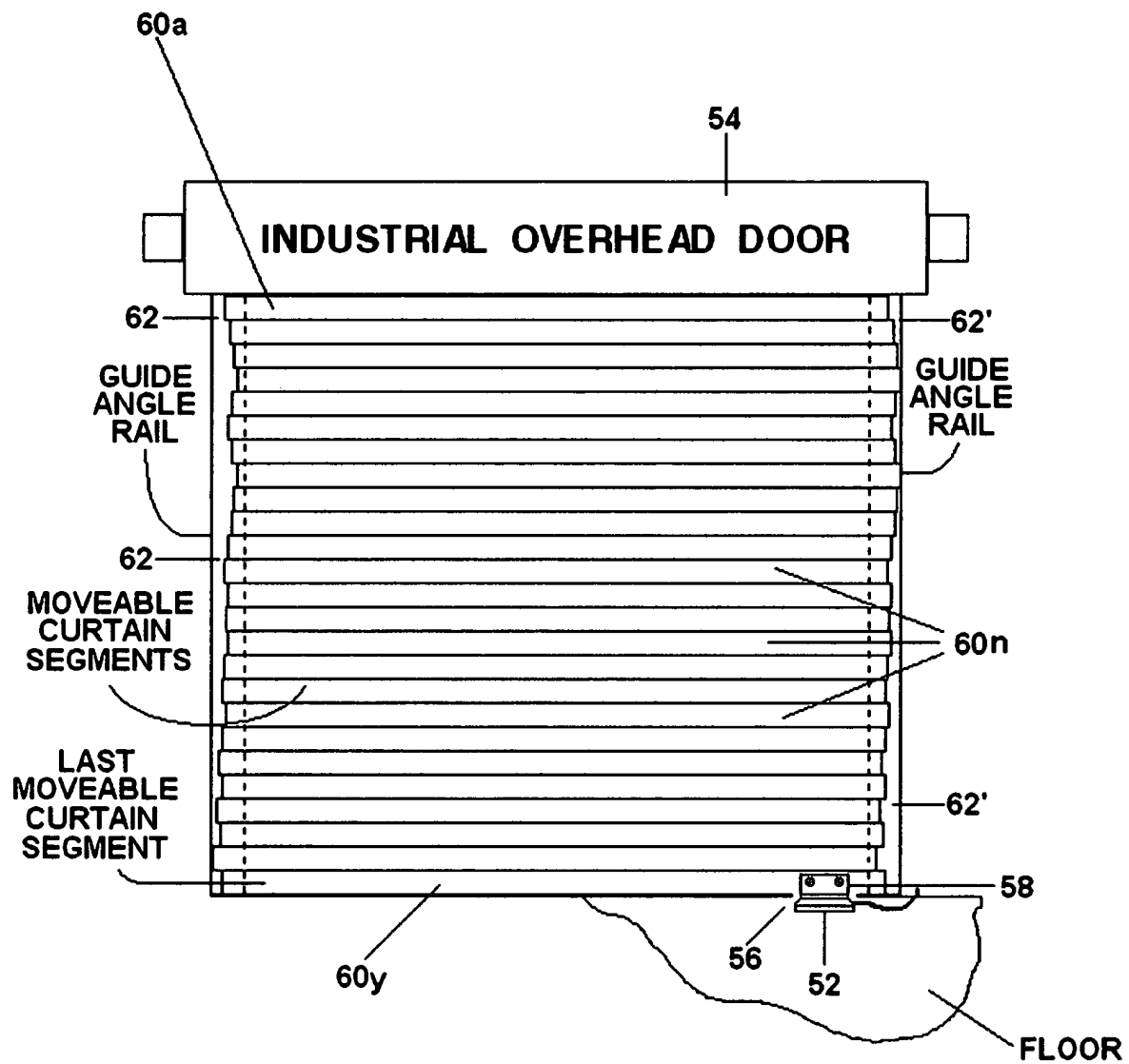
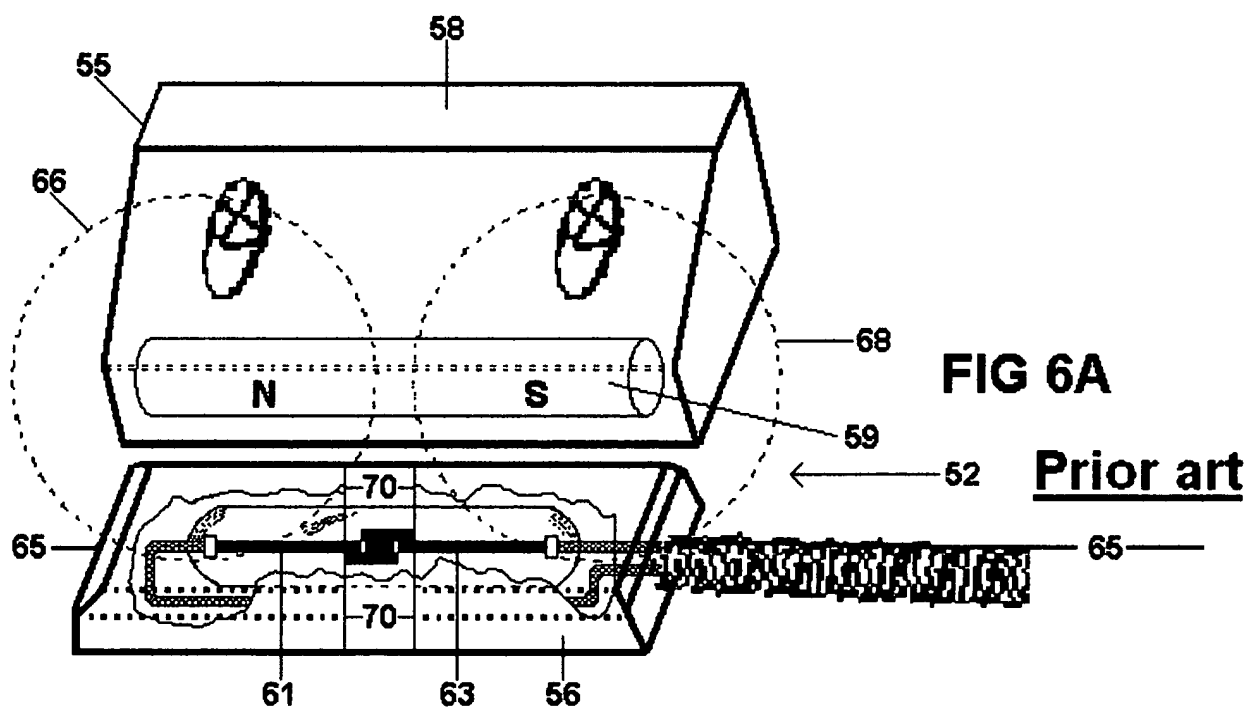
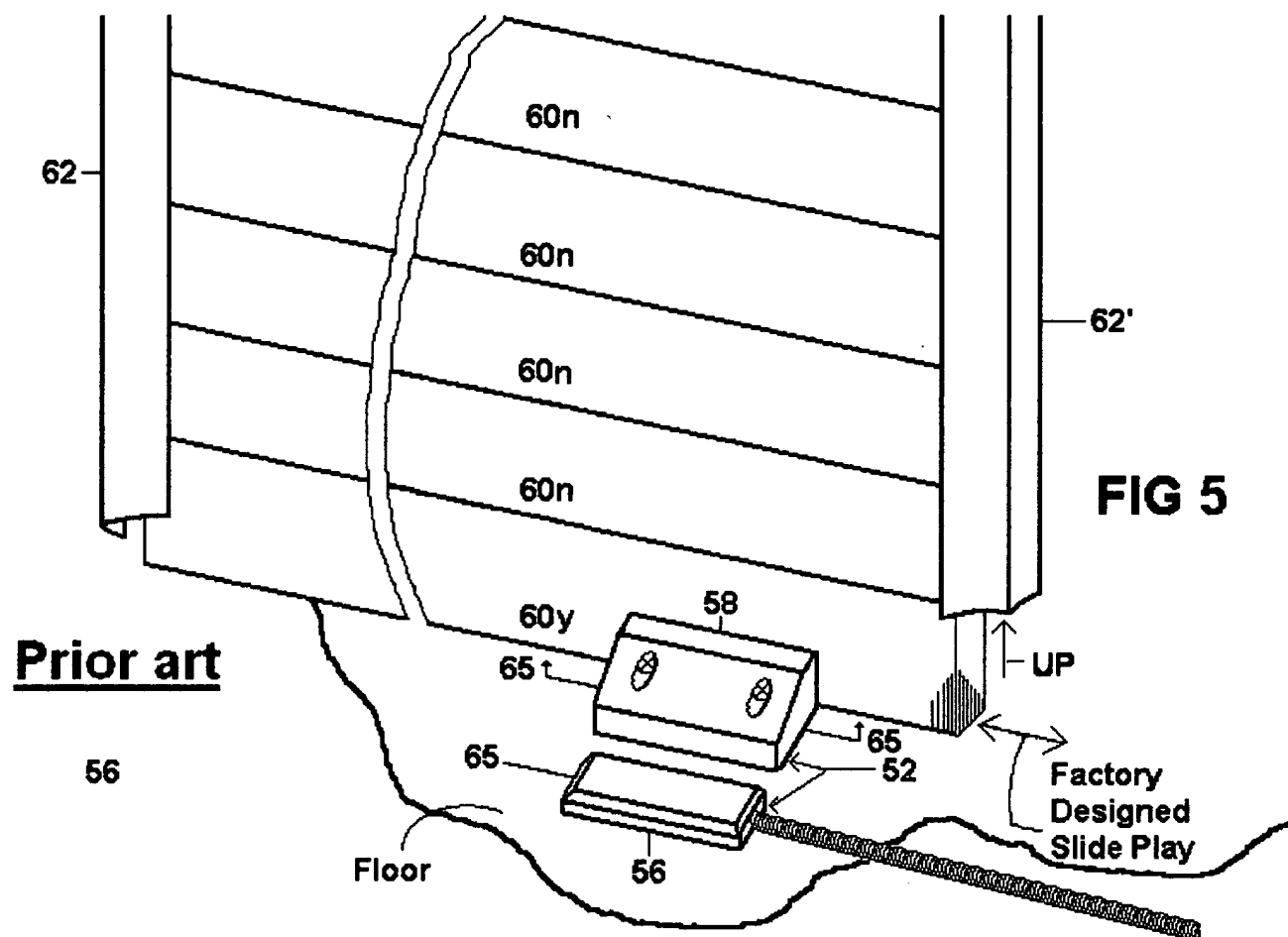


FIG 4. PRIOR ART



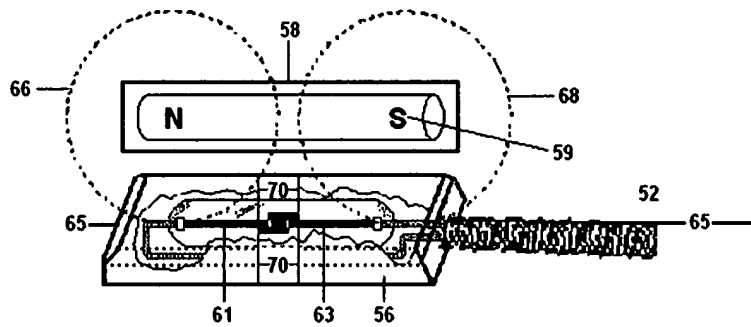


FIG 6B
Normal Circuit PRIOR ART

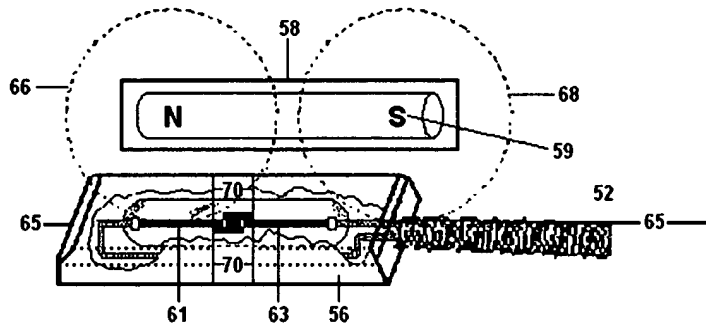


FIG 6C
Normal Circuit PRIOR ART

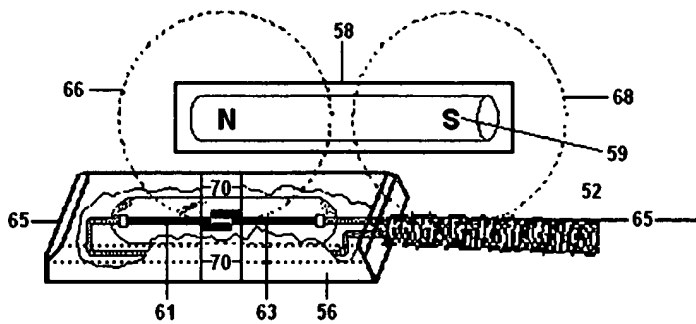
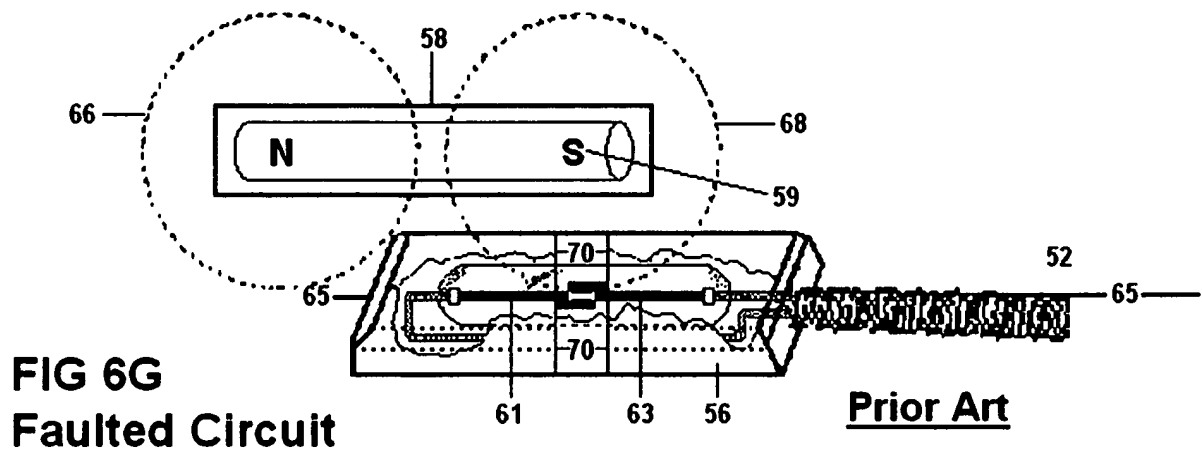
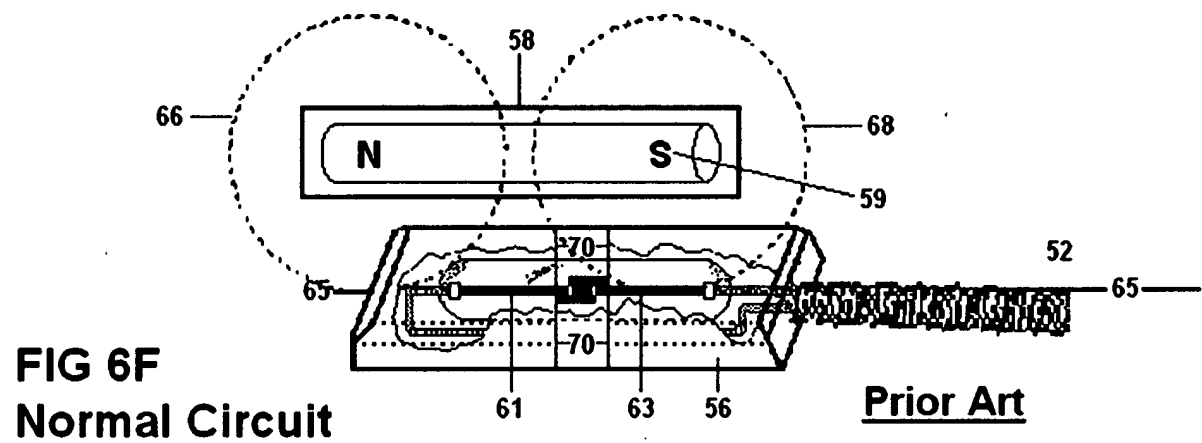
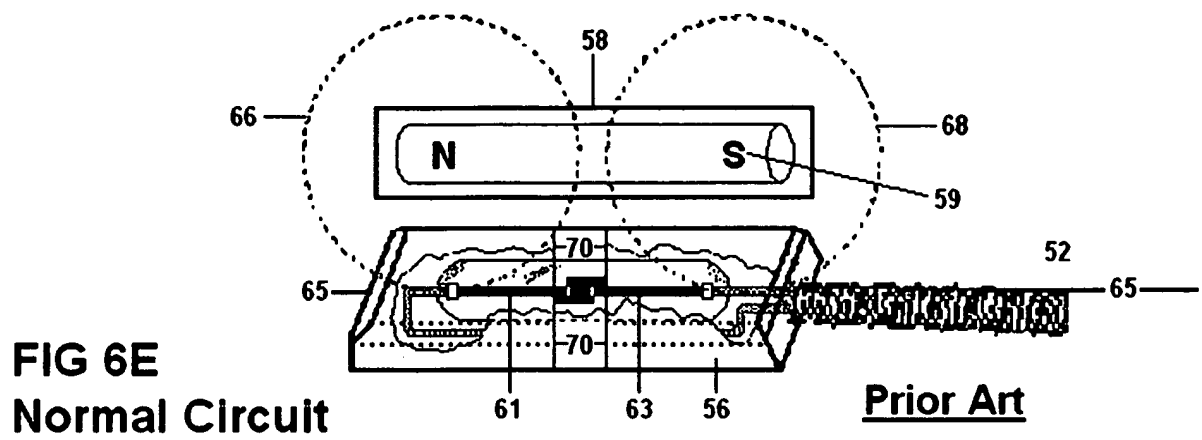
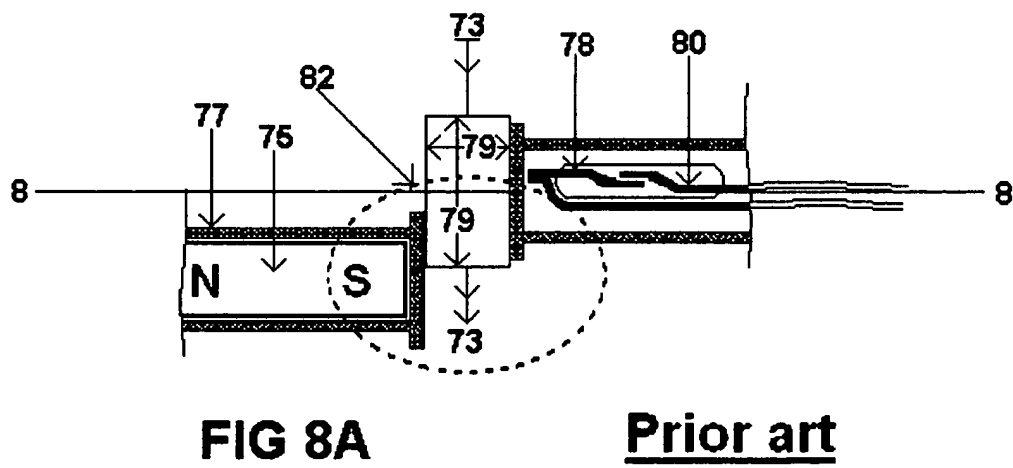
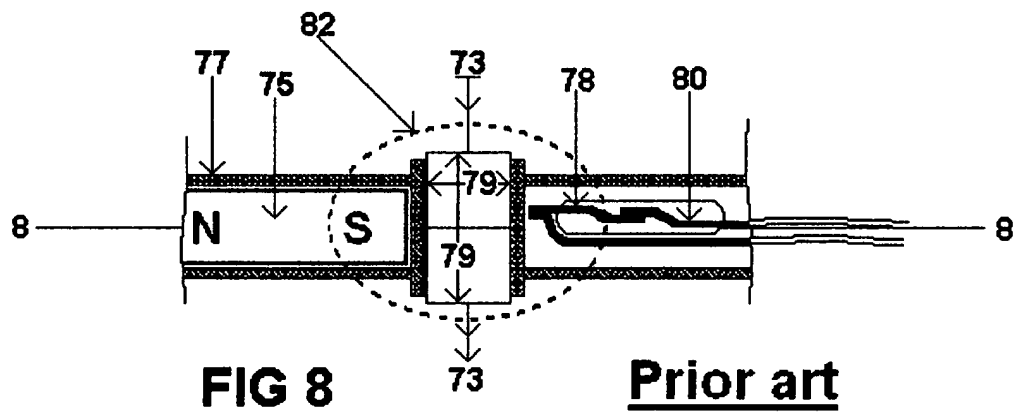
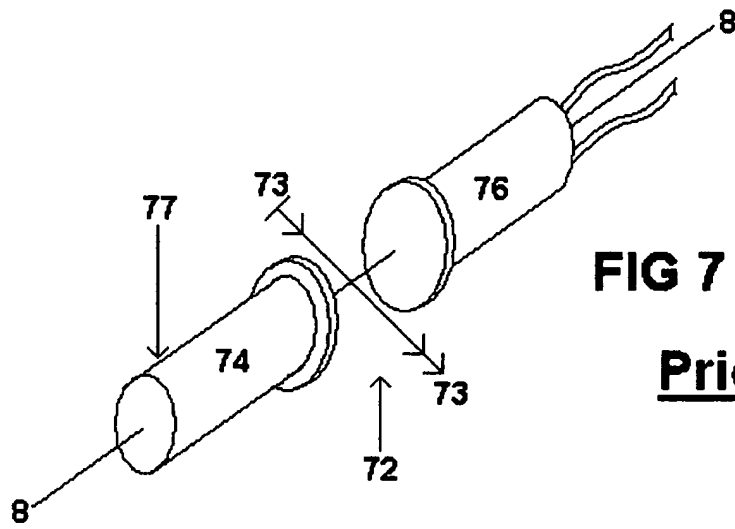


FIG 6D
Faulted Circuit PRIOR ART





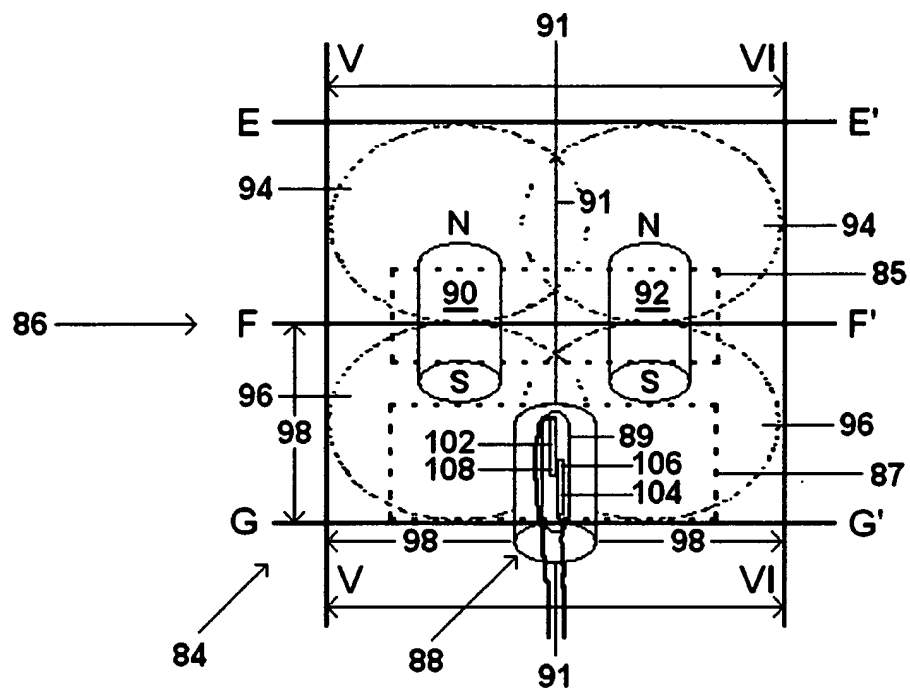


FIG. 9

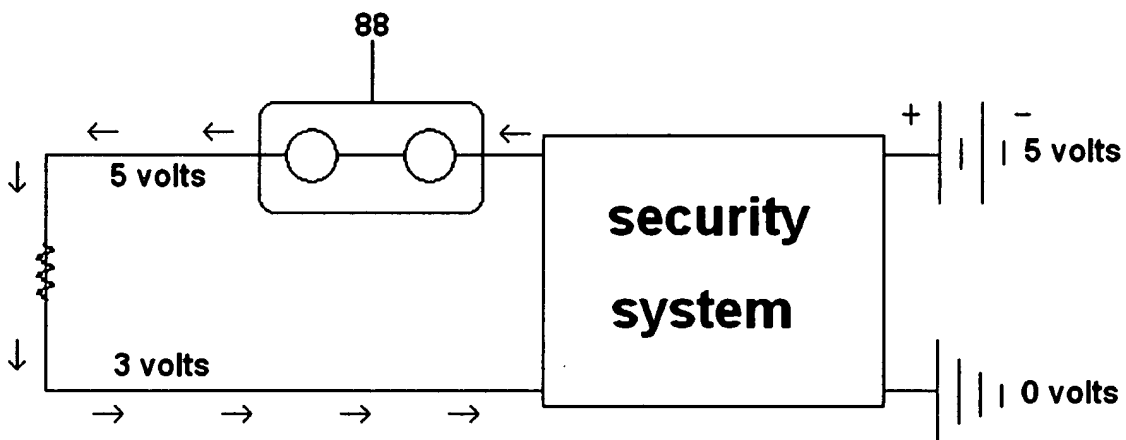
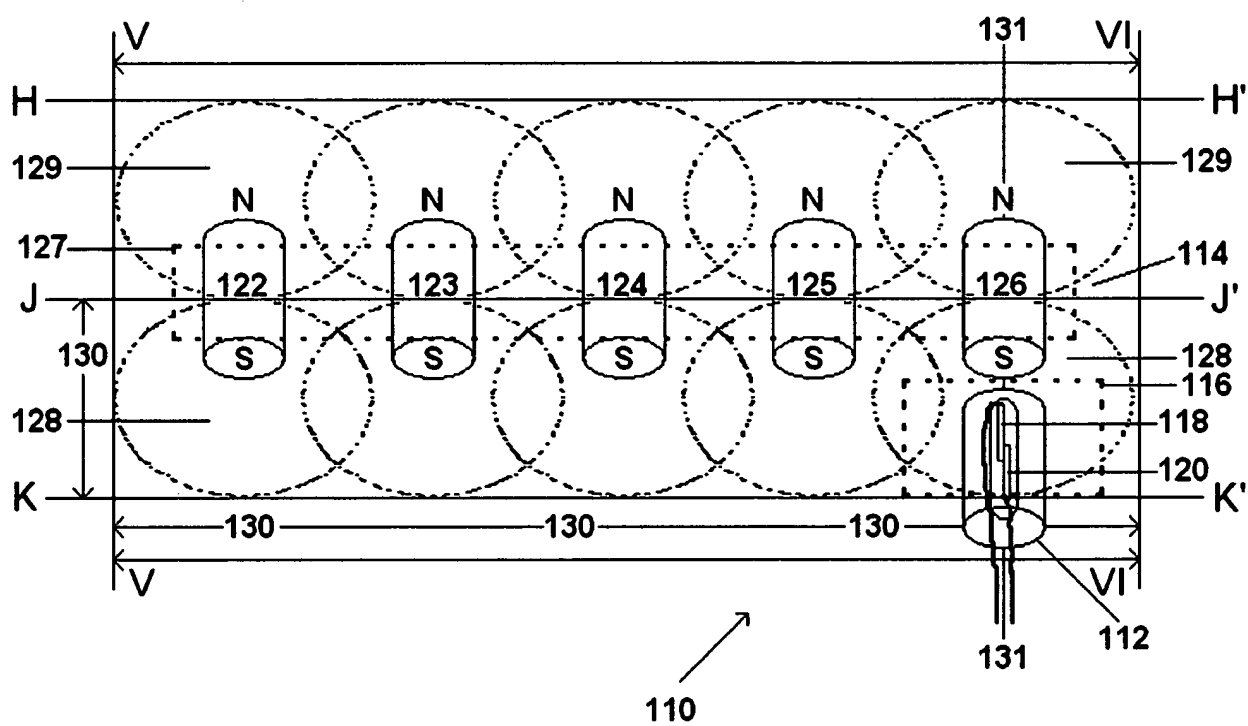


FIG 9A

FIG. 10



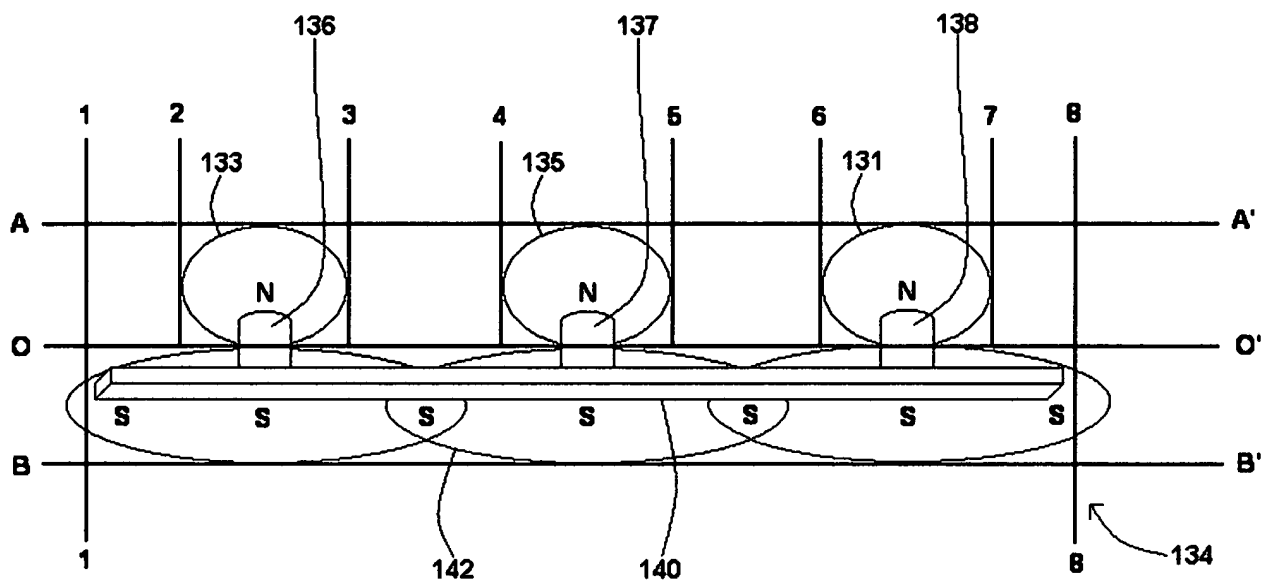


FIG 11

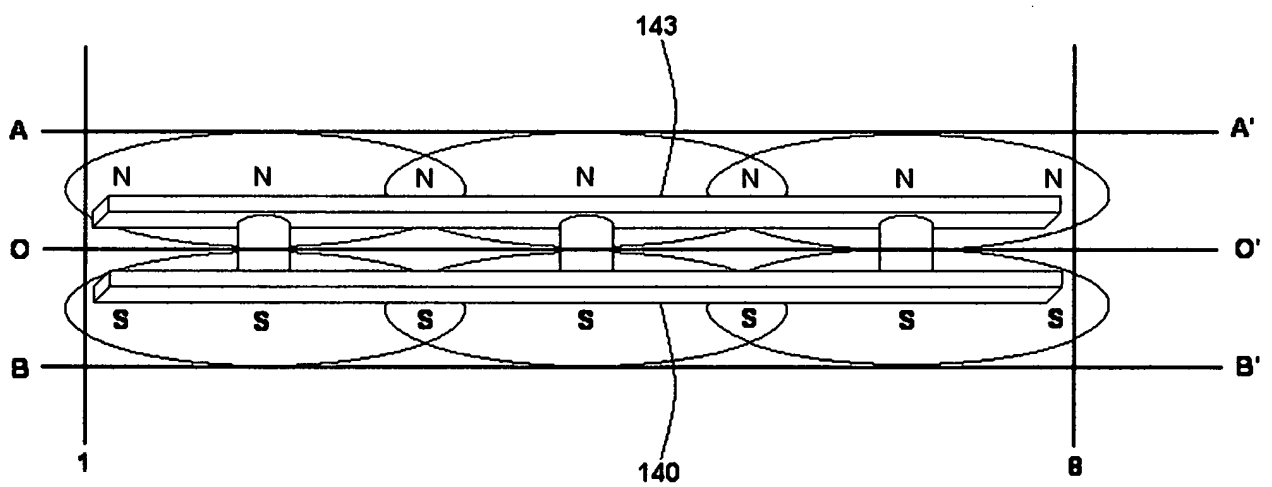


FIG 11A

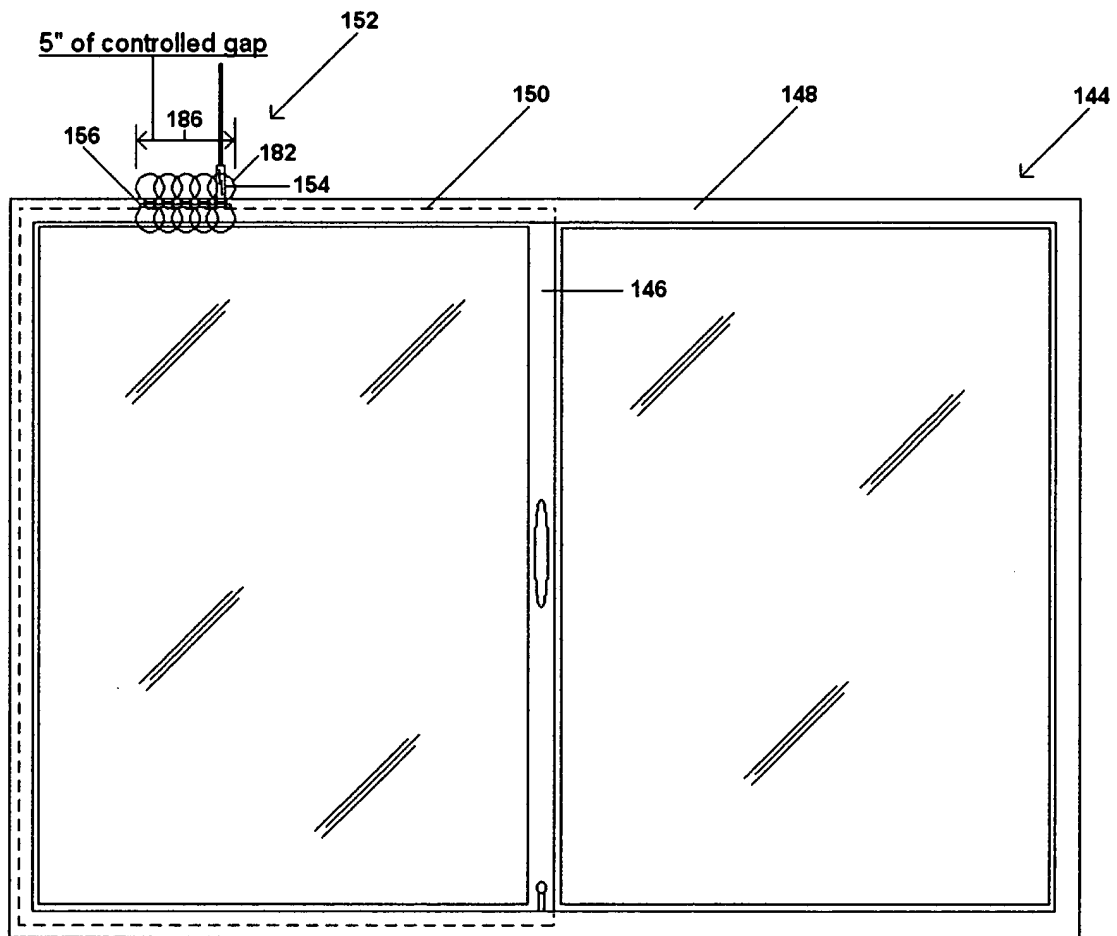


FIG. 12

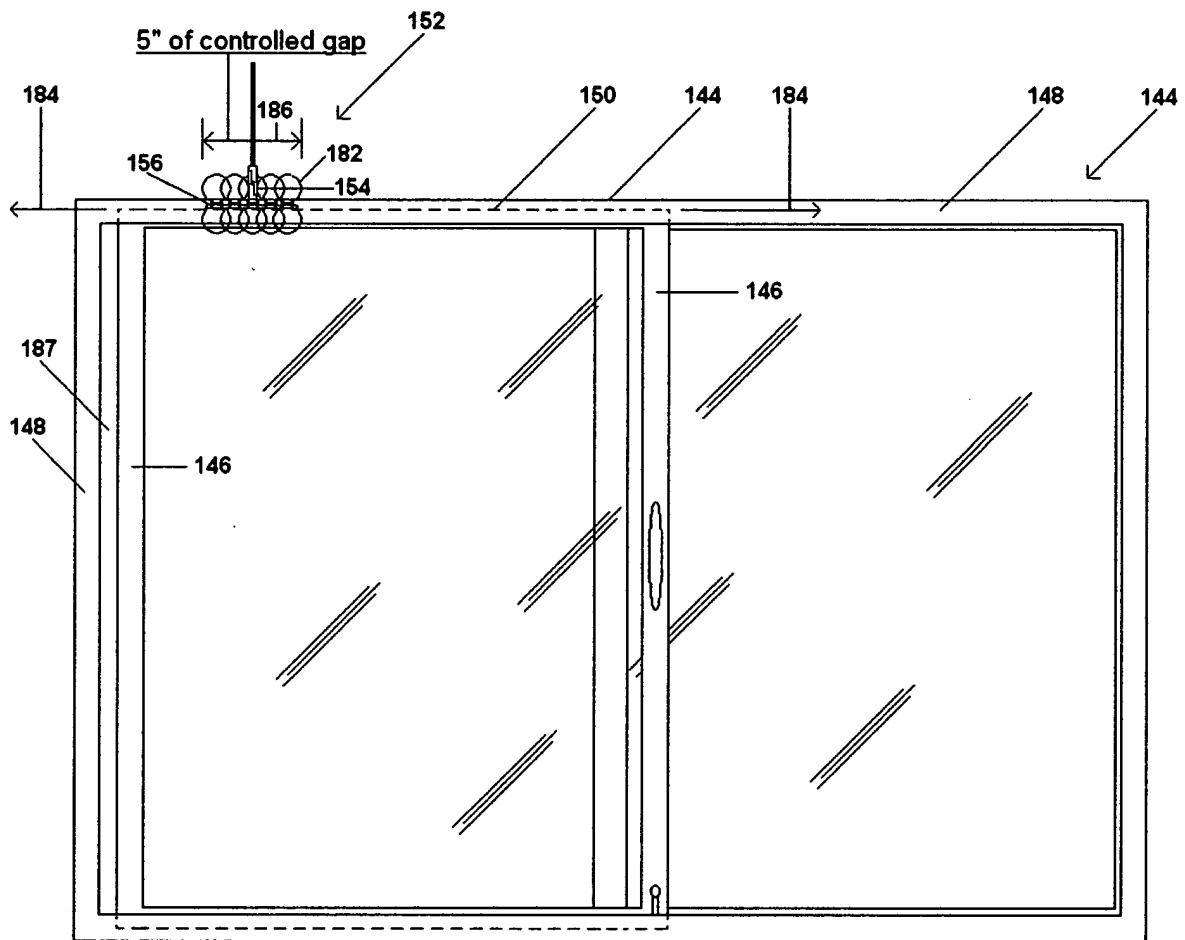


FIG. 14

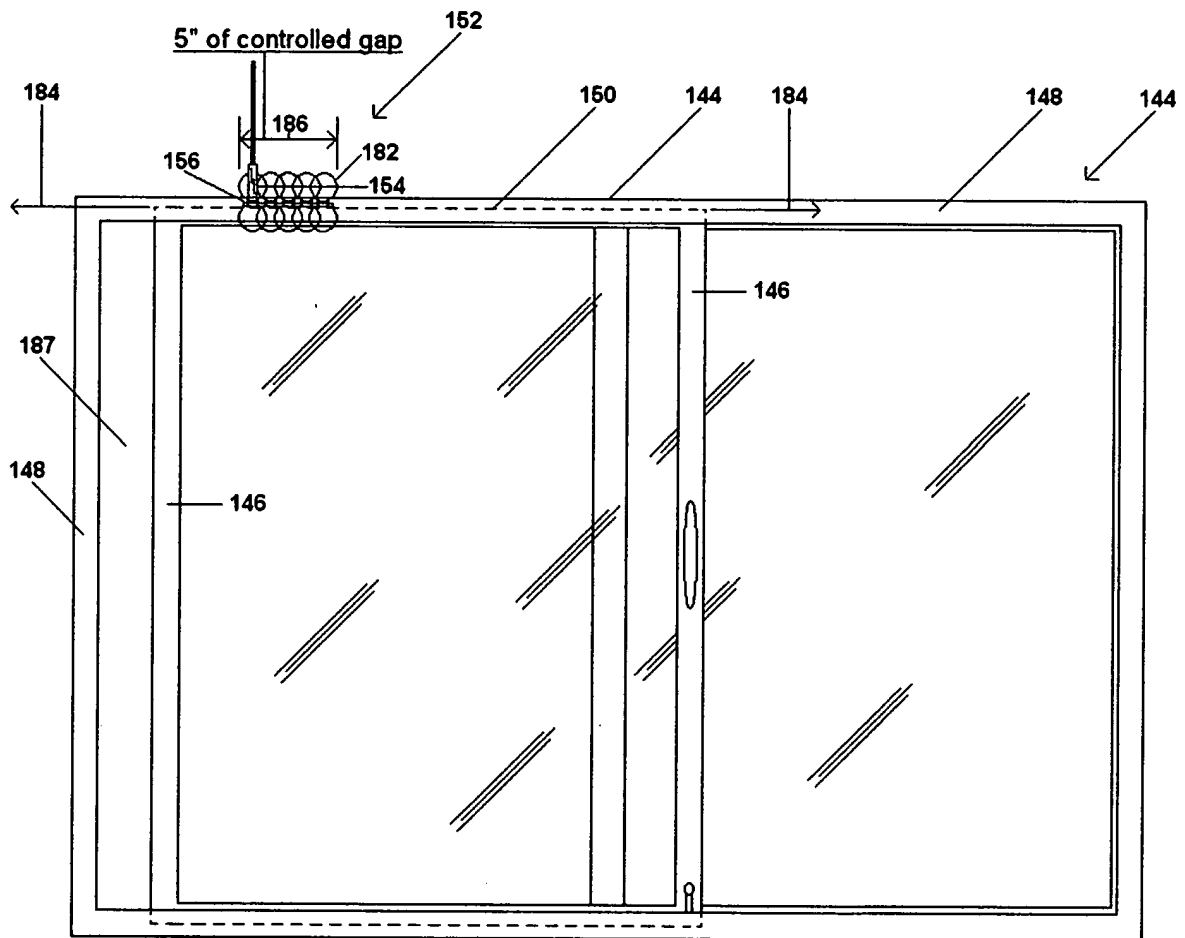


FIG. 15

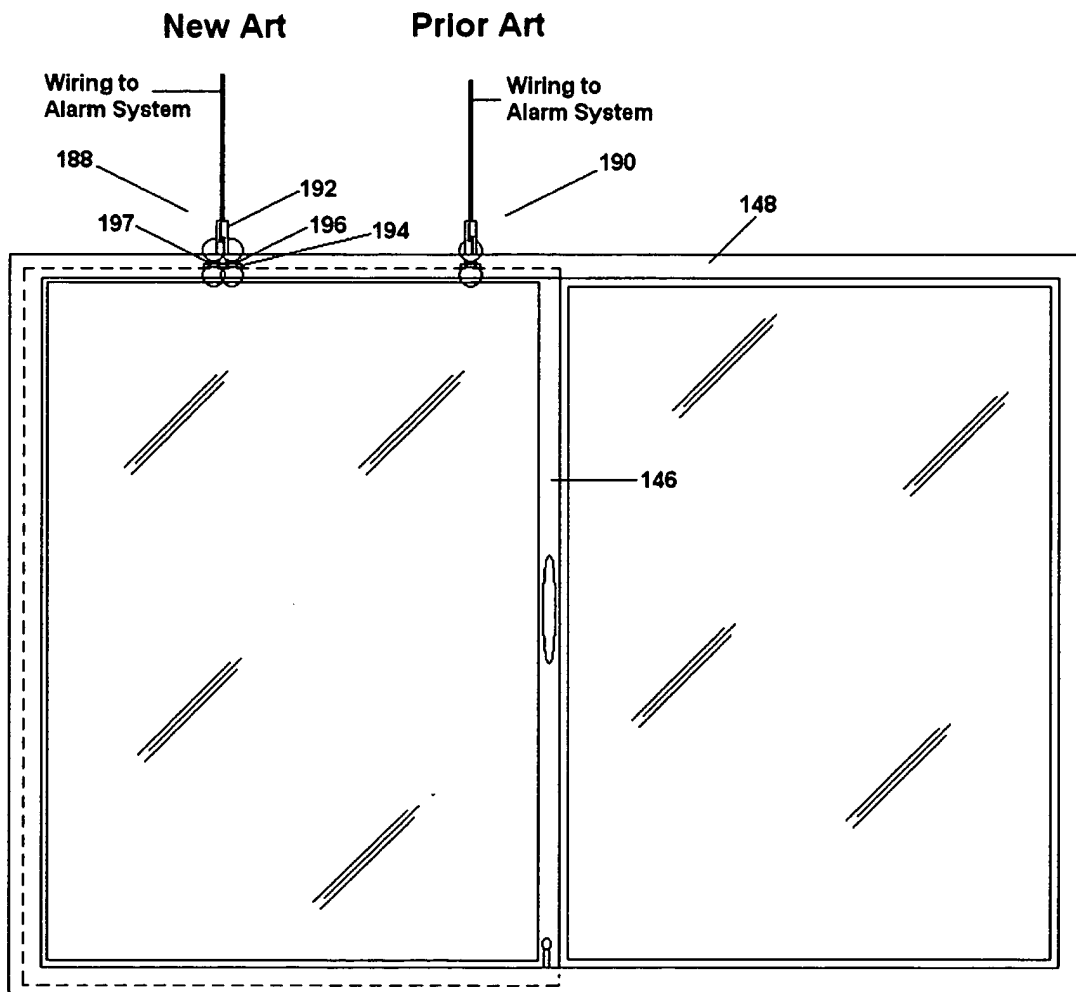


FIG.16

FIG. 17 **New Art** **Prior Art**

Prior Art

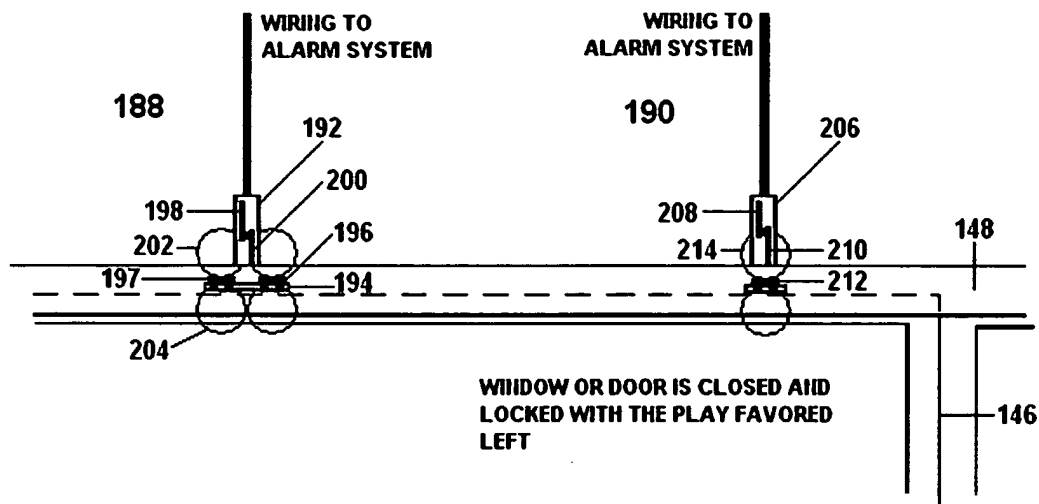
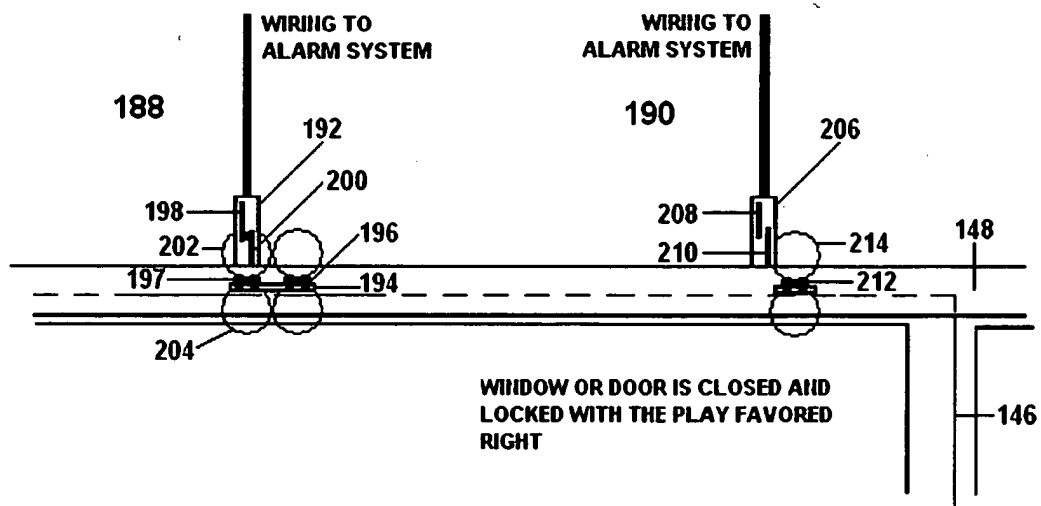


FIG. 18 **New Art**

Prior Art



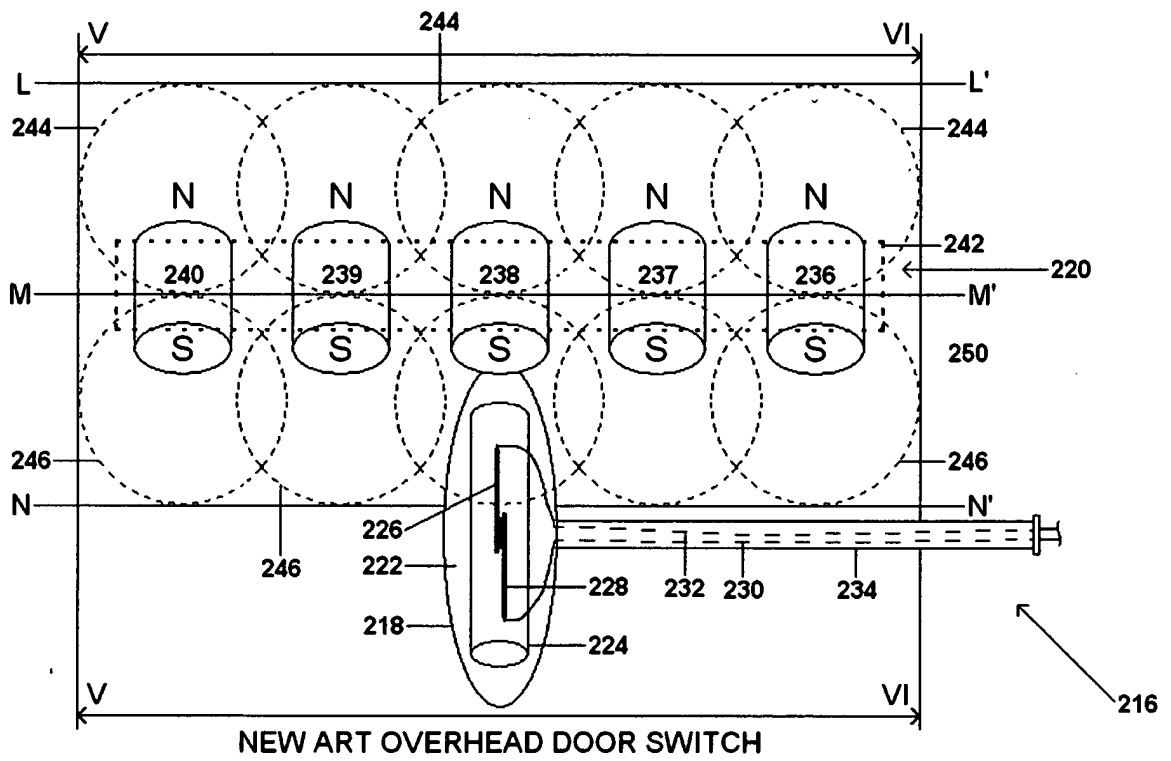


FIG. 19

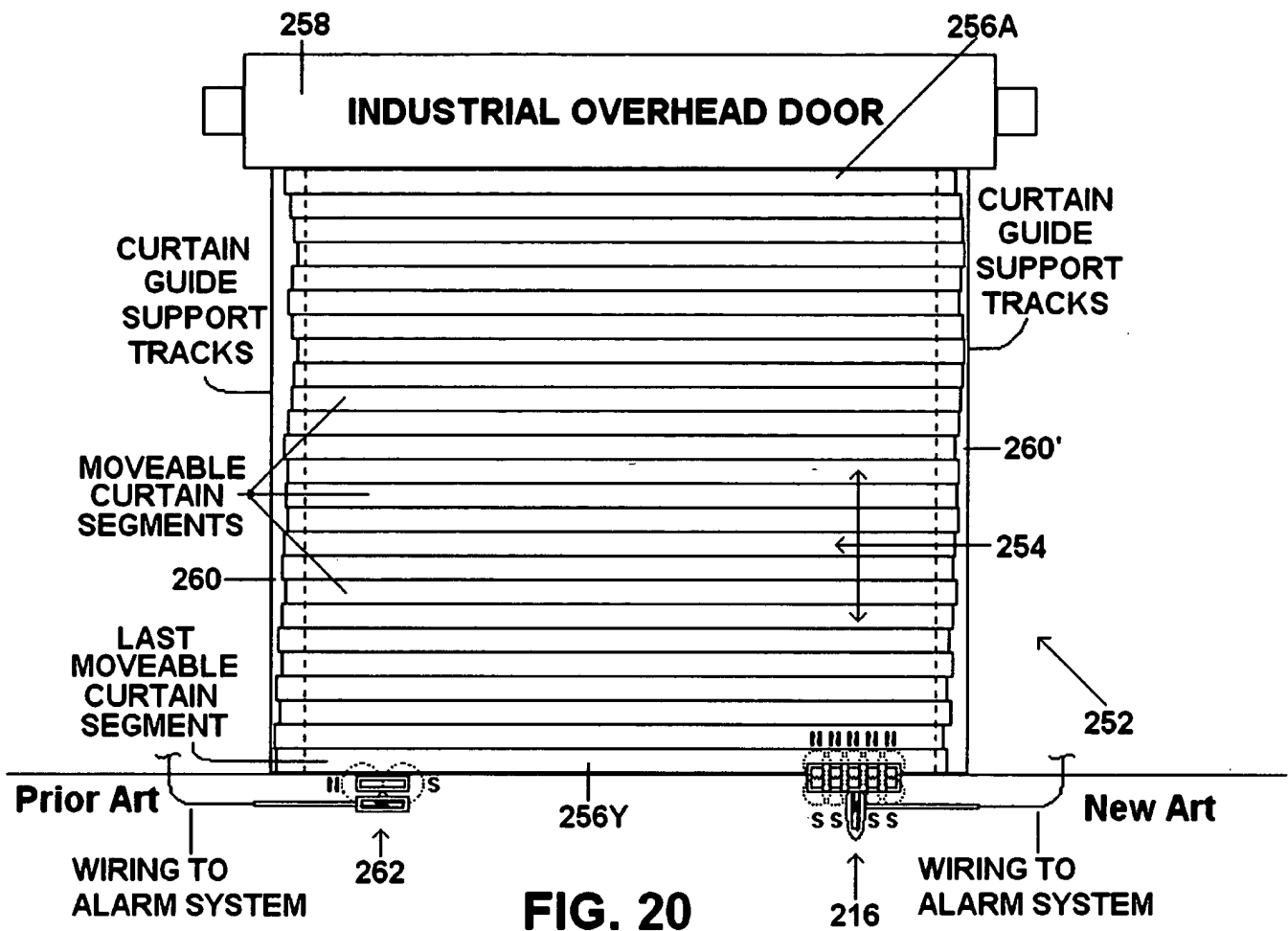


FIG. 20

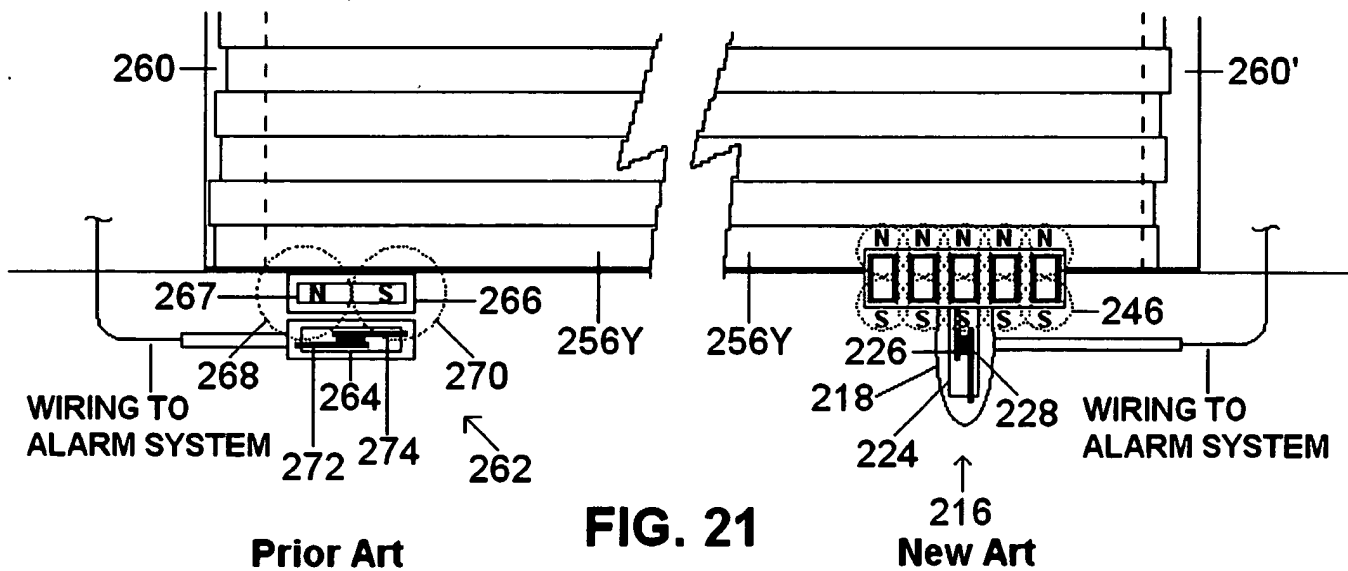


FIG. 21

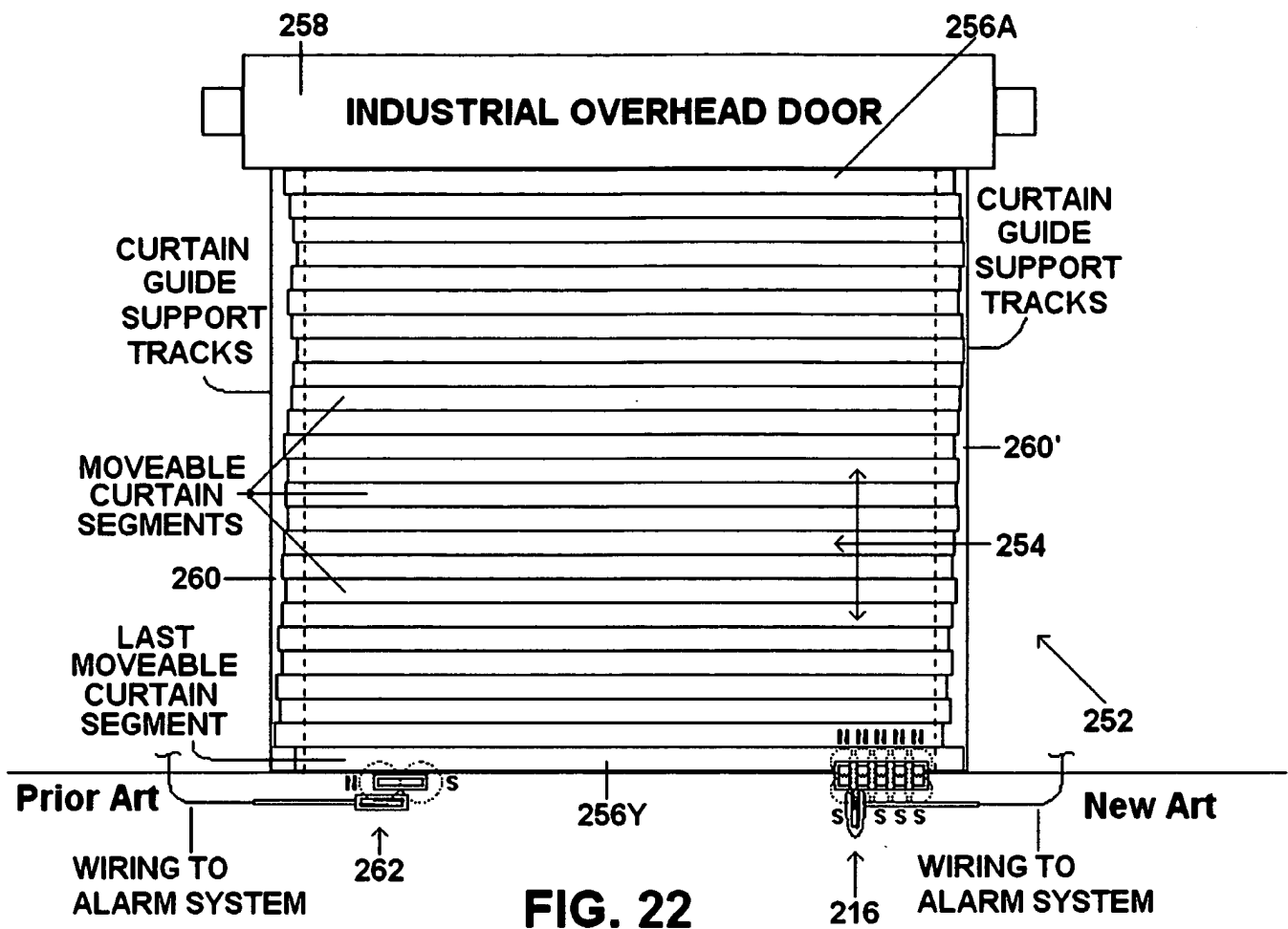


FIG. 22

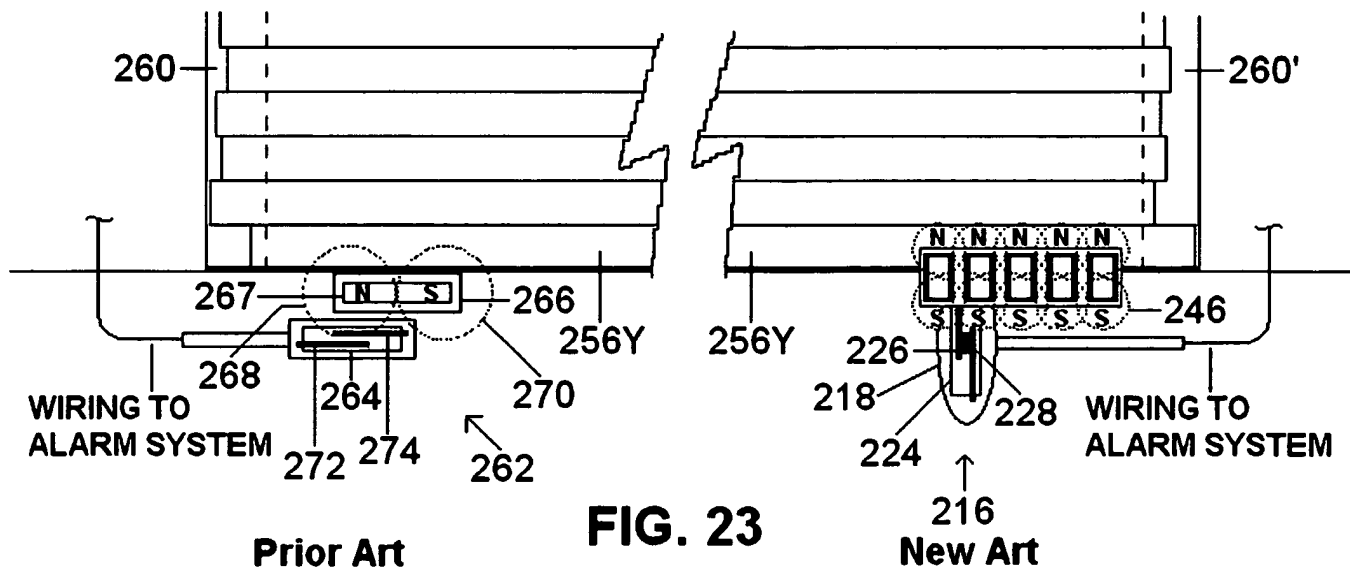


FIG. 23

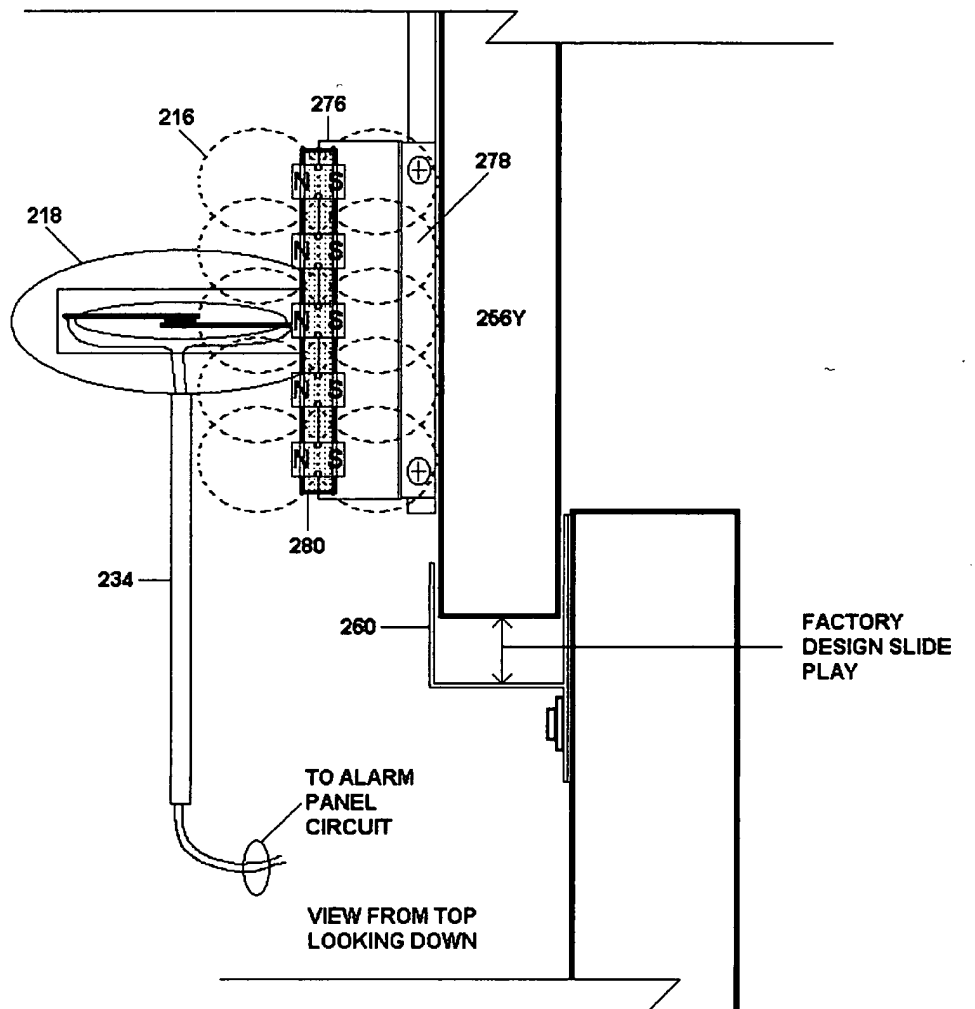


FIG. 24

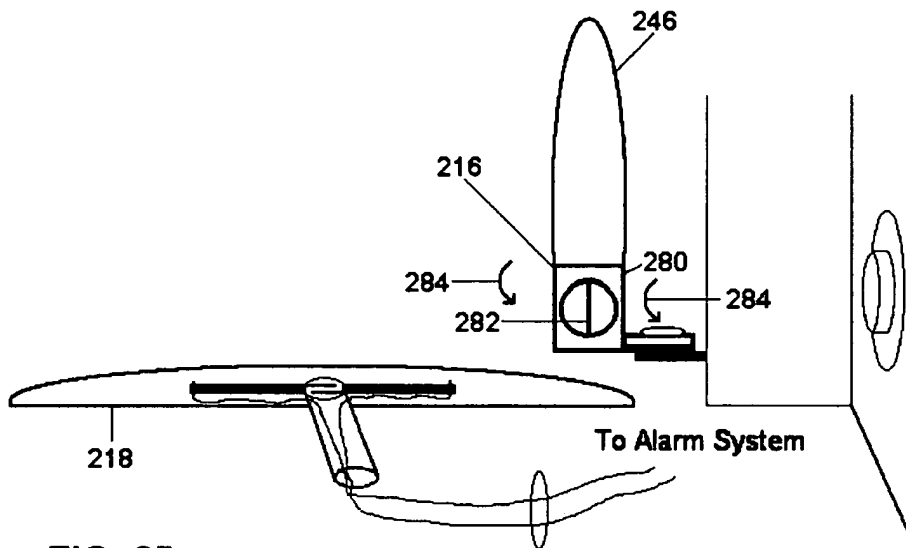


FIG. 25

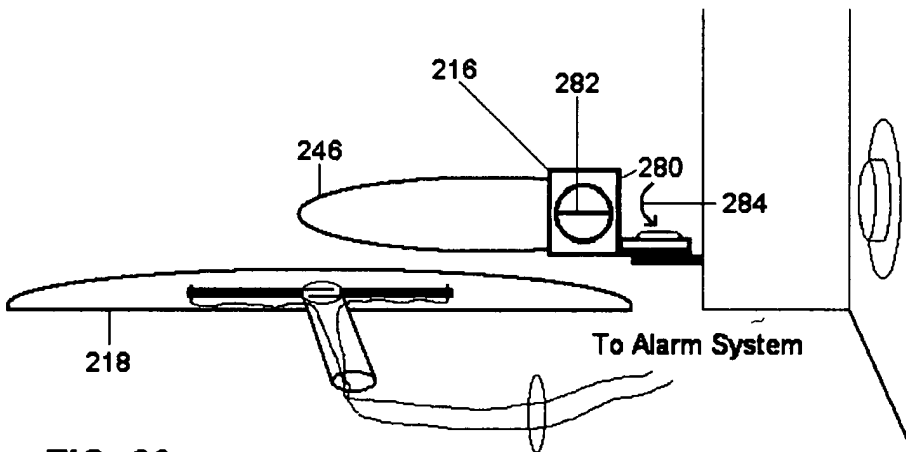


FIG. 26

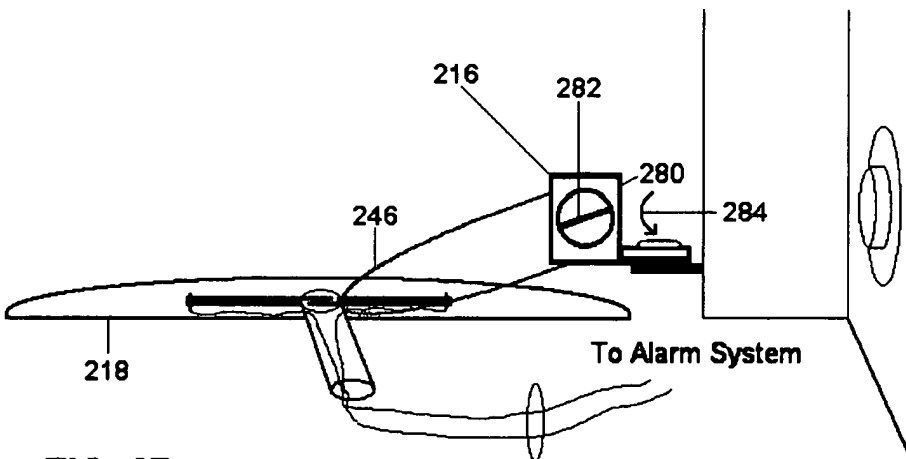


FIG. 27

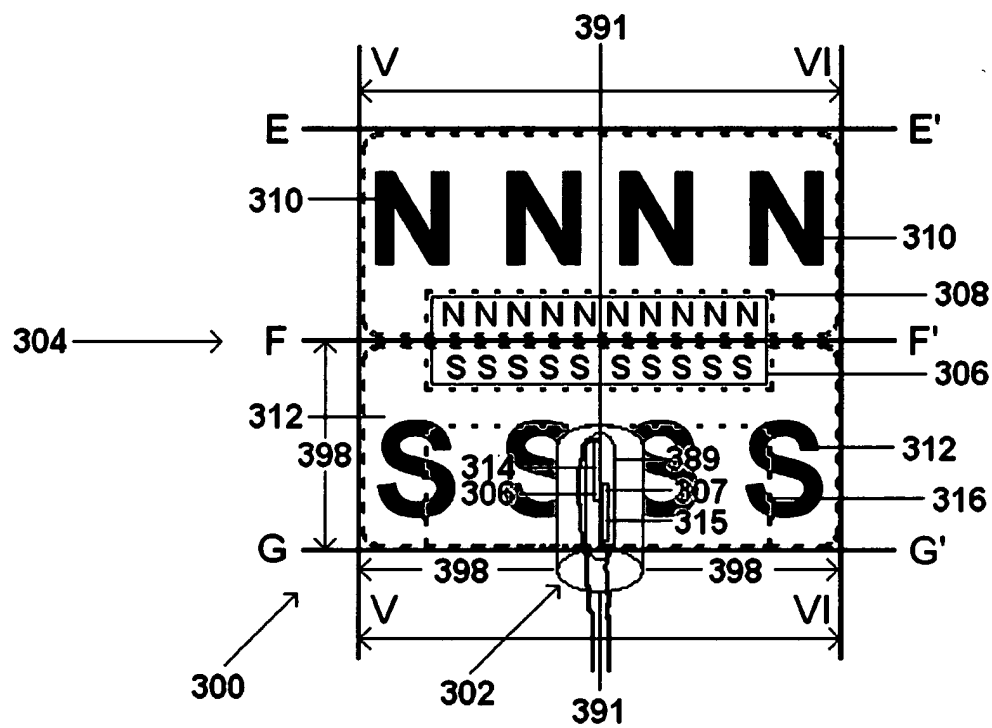
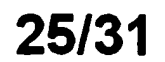


FIG. 28

320





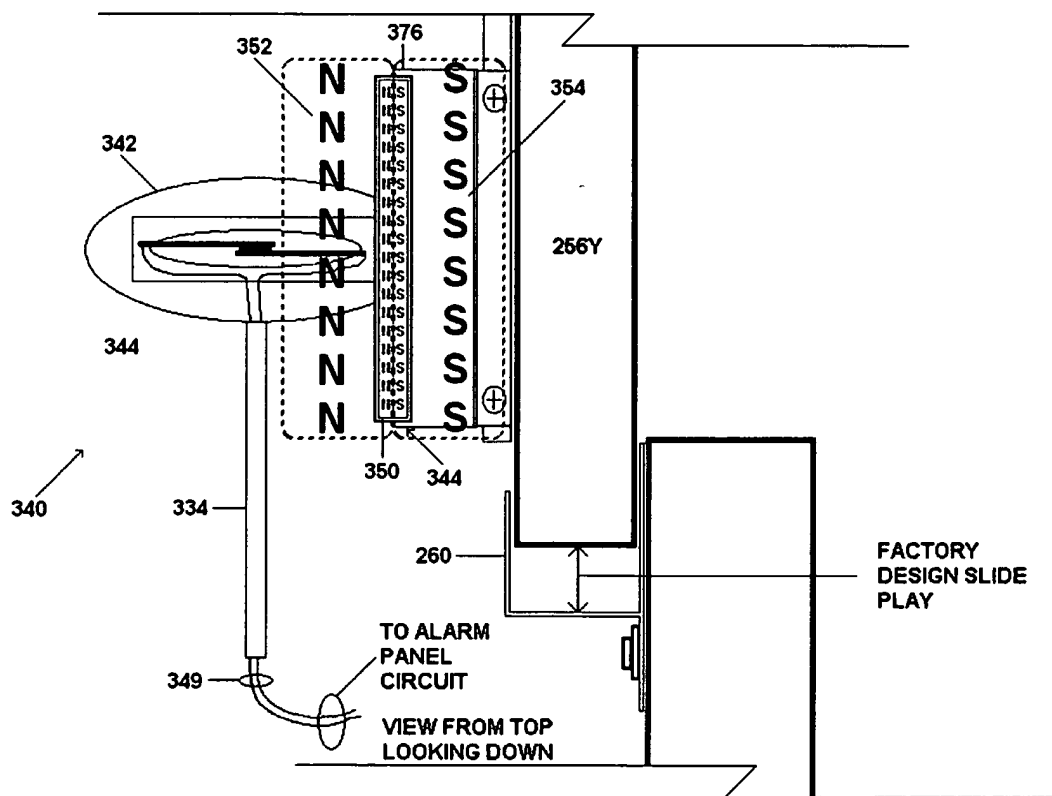


FIG. 31

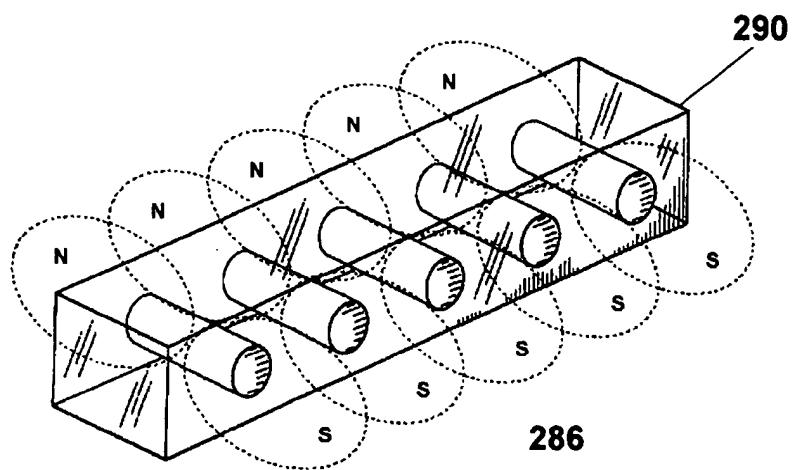


FIG. 32

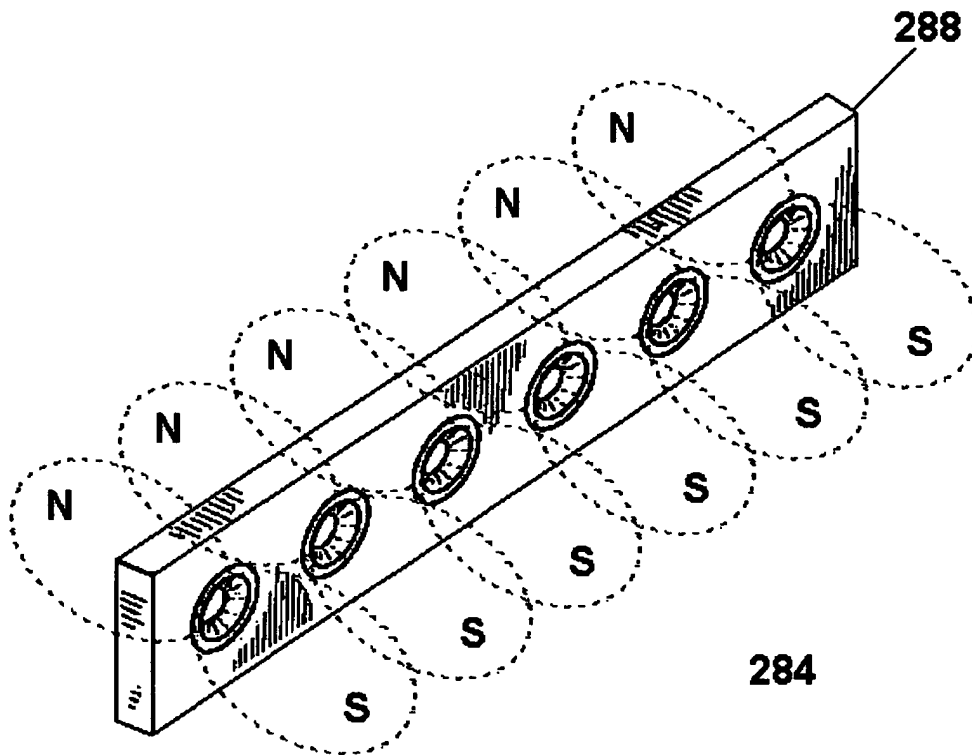


FIG. 33

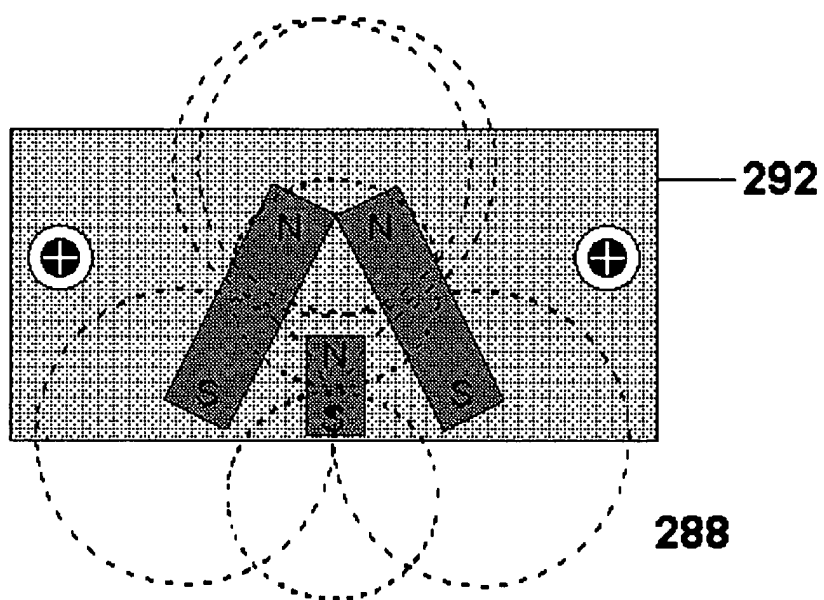


FIG. 34

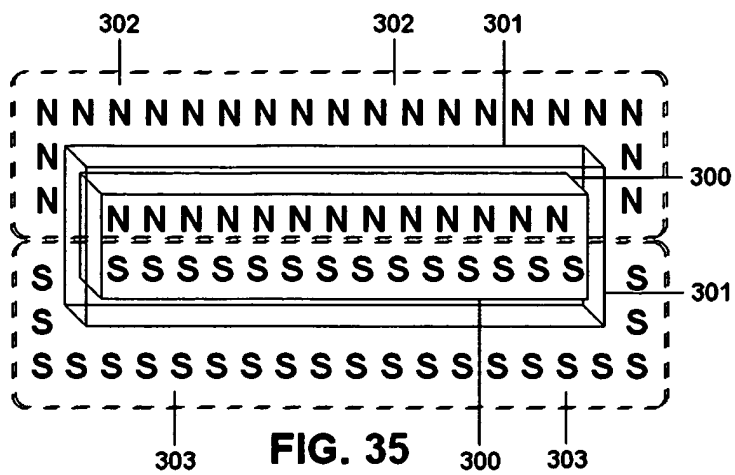


FIG. 35

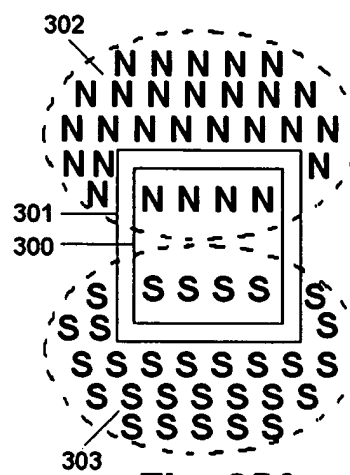


Fig. 35A

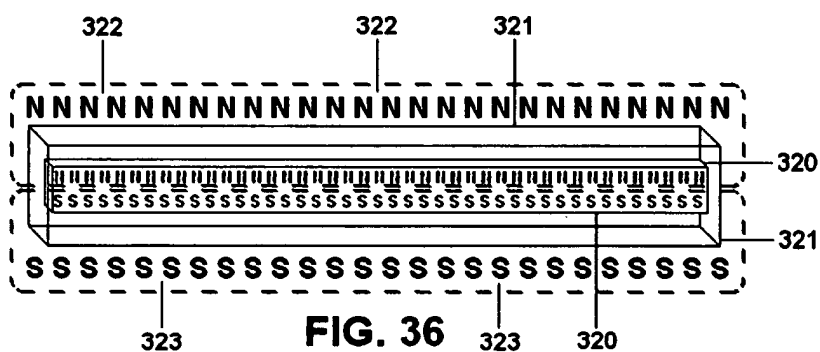


FIG. 36

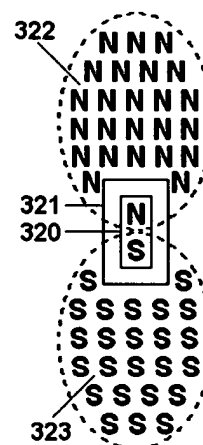


FIG. 36A

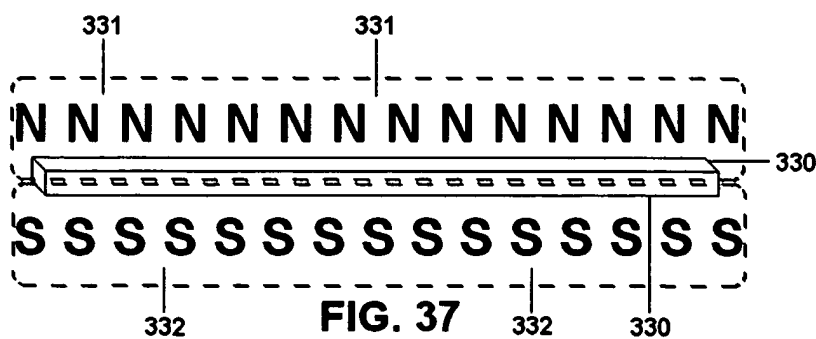


FIG. 37

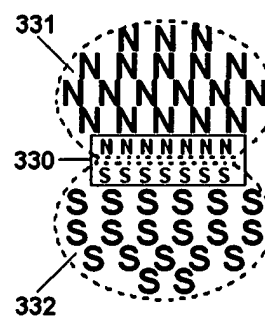


FIG. 37A